27.1 A 1/1.8-inch 6.4MPixel 60 frames/s CMOS Image Sensor with Seamless Mode Change

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Compact digital cameras require high pixel-count, high imaging-performance, and low power consumption. Pixel-size miniaturization is necessary to achieve a high pixel-count in an adequate optical format. Among CMOS image sensors, transistor-sharing techniques are widely used to make small pixels have better imaging performance [1, 2, 3]. The advantages of a CMOS image sensor are low power and easy system integration. Using these advantages, high-speed CMOS image sensors with on-chip ADC are developed [4, 5]. High-speed imaging is one of the promising applications for CMOS image sensors.

A 6.4MPixel 60frames/s CMOS image sensor is developed. The sensor is fabricated using a 0.18μm 1P3M process. Zigzag-shaped 1.75transistor/pixel architecture enables 2.5×2.5μm^2 pixels of high saturation and sensitivity. Column-parallel counter-type 10b ADCs are operated at a data rate of 432MHz enabling 6.4MPixels at 60frames/s. Moreover, a 6.4MPixel readout and 2×2 binning modes are interchangeable without insertion of an invalid frame to avoid integration-time inconsistency.

Figure 27.1.1 shows the block diagram of the sensor. The sensor consists of a pixel block, a column-parallel counter-type 10b ADC, control logic, and peripheral circuits including a PLL, generating 432MHz counter clock from a 54MHz input clock. The column-parallel ADCs are composed of column-parallel comparators, counters and latches. A 10b/12b parallel LVDS interface circuit is chosen enabling data rates up to 432MHz.

Figure 27.1.2 shows the pixel arrangement. A Zigzag-shaped 4-pixel sharing technique is employed. The resulting transistor count is 1.75transistor/pixel. The upper 2 pixels share the first floating diffusion. The second floating diffusion is shared by the lower 2 pixels. The first and second floating diffusion areas are connected together by wiring. A conversion gain of 40μV/e is achieved by optimizing the layout. By using zigzag-shaped sharing, an optical aperture ratio of 38% (without on-chip microlenses) and handling capacity of 12,000e at 60˚C are realized. A Bayer-pattern color filter and a microlens are fabricated on-chip. The measured quantum efficiency and sensitivity of the green pixels are 48% at 550nm and a sensitivity of 14,000e/lux*s.

In this configuration, the deviation of both the Gr and Gb pixel signals becomes negligible, because the Gr and Gb photodiodes share the same transistors and the same column circuits. Moreover, the single shared unit has the same color pixels and charge summing at floating diffusion can be possible.

Figure 27.1.3 shows readout sequence of this sensor. The horizontal scanning time is set to 7.2μs allowing 6.4MPixels at 60frames/s. During the first period before the transfer pulse TRn, the reset level of the pixel is read out to the vertical signal line (VSL). Additionally, the ramp signal (Vcomp) is supplied to column comparators and down-counting is carried out to latch the reset level of the pixel. After transferring the signal charge (the second period), the signal level of the pixel is read out again. The ramp signal (Vcomp) is again supplied to the column comparators. At this time, the counting direction is changed from down to up. Over the course of both the first and the second periods, digital CDS operation is accomplished. This results in an FPN-subtracted signal.

Both readout of the previously selected row and A/D conversions of the currently selected row are performed simultaneously.

The A/D conversion is accomplished during this up and down counting. Therefore, by repeating these counting actions, signals from 2 rows of pixel can be digitally mixed. In Fig. 27.1.4, signals from nth and n+2th rows are digitally converted together using this method. The resulting data is the summation of the nth and n+2th rows. Signal mixing in the horizontal direction is done using output control circuits. In this sensor, the 6.4MPixel mode and 2×2 (1.6MPixel) modes are interchangeable. This is done without an extra frame to adjust integration time mismatch between two modes. In conventional CMOS image sensors, it is necessary to insert an invalid frame to obtain a certain integration time for various readout modes. This is because the integration time of adjacent color rows is different between two modes.

The total count of the ramp signal (Vcomp) determines the ADC resolution of this sensor. A readout of 6.4MPixels at 60frames/s requires a horizontal scanning time of 7.2μs and an ADC resolution of 10b. 12b resolution is also available if 15frames/s are chosen. In this mode the data rate is lowered to 108MHz.

Specifications and characteristics are summarized in Fig. 27.1.5. An Input clock of 54MHz is required to obtain a 432MHz data rate using an embedded PLL. The sensor also has a draft mode, in which 1/5 of vertical rows is read out, in addition to 6.4MPixel and 2×2 modes. This draft mode results in a frame rate of 300frames/s. Saturation of 12,000e is achieved without image lag. Measured random noise is 7e. Power consumption is 360mW when supply voltage is 3.0V/1.8V. A reproduced image and the chip micrograph are shown in Fig. 27.1.6 and Fig. 27.1.7, respectively.

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References:
[1] H. Takahashi, et al., "A 3.9μm Pixel Pitch VGA Format 10b Digital Image Sensor with 1.5-Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 108-109, Feb., 2004.
[2] M. Mori, et al., "A 1/4in 2M Pixel CMOS Image Sensor with 1.75 Transistor/Pixel," *ISSCC Dig. Tech. Papers*, pp. 110-111, Feb., 2004.
[3] K. Mabuchi, et al., "CMOS Image Sensor Using a Floating Diffusion Driving Buried Photodiode," *ISSCC Dig. Tech. Papers*, pp. 112-113, Feb., 2004.
[4] A. Krymski, et al., "A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS Sensor," *IEEE Trans. Electron Devices*, vol. 50, pp. 130-135, Jan., 2003.
[5] Y. Nitta, et al., "High Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low Noise APS," *ISSCC Dig. Tech. Papers*, Paper 27.5, Feb., 2006.

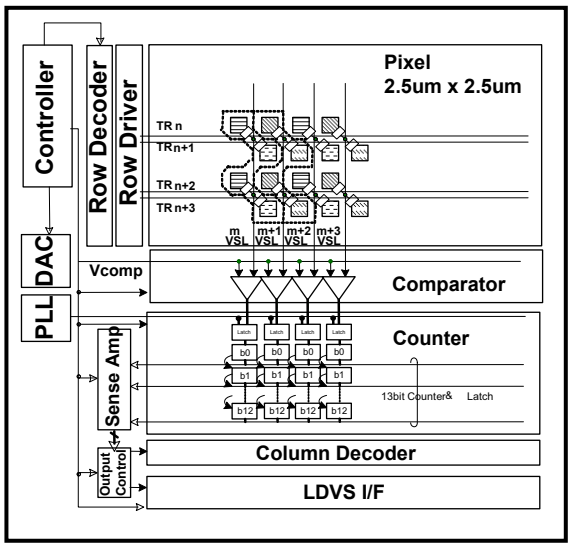

Figure 27.1.1: Block diagram.

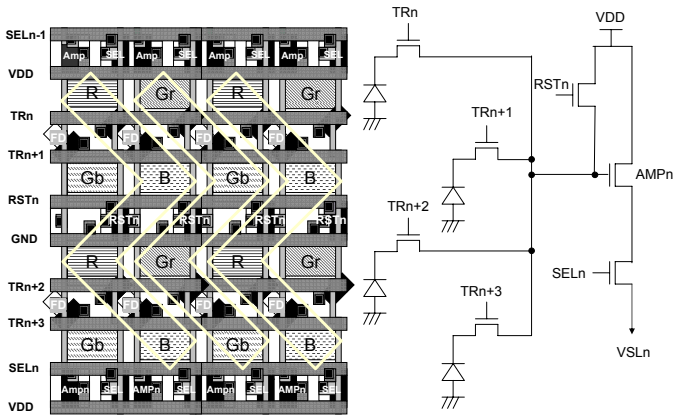

Figure 27.1.2: Pixel arrangement.

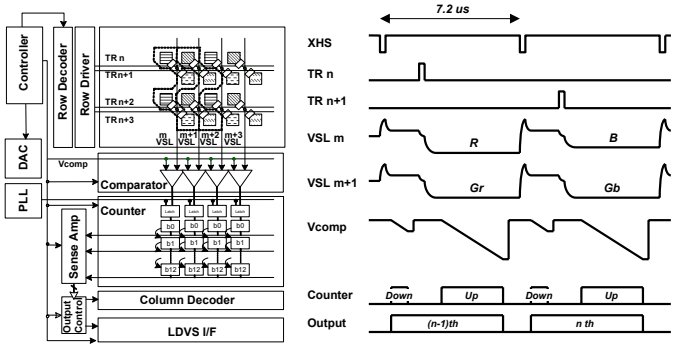

Figure 27.1.3: Readout sequence (6.4MPixel).

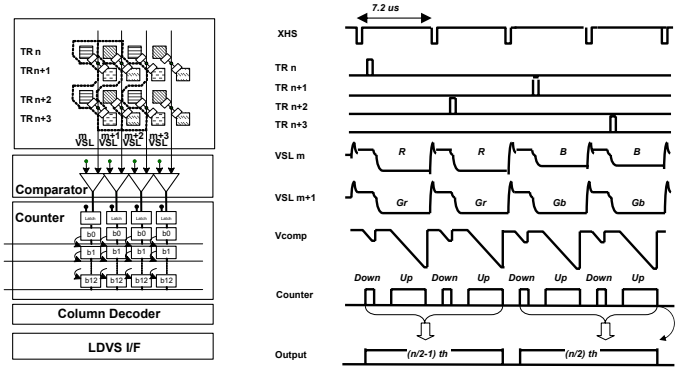

Figure 27.1.4: Readout sequence (2×2 binning).

Specification

Item	Data
Process	0.18um 1P 3M
Pixel size	2.5um (H) X 2.5um (V)
Number of effective pixels	2928 (H) × 2184 (V)
Aperture ratio	38% without on-chip microlens
Supply voltage	3.0V / 1.8V
Input clock rate	54MHz
Max. Data rate	432MHz (216MHzDDR)
Output	12bit parallel LVDS
Mode	6.4Mpixel 60frames/s *1
	1.6Mpixel(2×2) 60frames/s *1
	1.2Mpixel (1/5 line readout) 300frames/s

*1 Seamless mode change

Characteristics

Item	Data
Quantum Efficiency	48% (at 550nm)
Sensitivity	14,000 electrons / lx*s At 3200K light source with IR cut filter of 650nm cut-off
Saturation signal	12,000e at 60C
Lag	Below measurement threshold
Dark current	15e/s at 60C
RMS Random Noise	7e rms At 60frames/s, Gain 0dB
RMS Vertical FPN	0.7e rms At 60frames/s, Gain 0dB
Dynamic range	64.7dB at 60frames/s
ADC resolution	10 bit at 6.4M 60frames/s 12bit at 6.4M 15frames/s
ADC INL	4LSB
ADC DNL	<0.5LSB
Conversion gain	40uV/e
Power consumption	360mW at 60frames/s

Figure 27.1.5: Specification and characteristics.

Conditions

Mode	**6.4Mpixel**
Frame rate	**60frames/sec**
Integration time	**16.6msec**
Analog Gain	**0dB**

Figure 27.1.6: Reproduced image.

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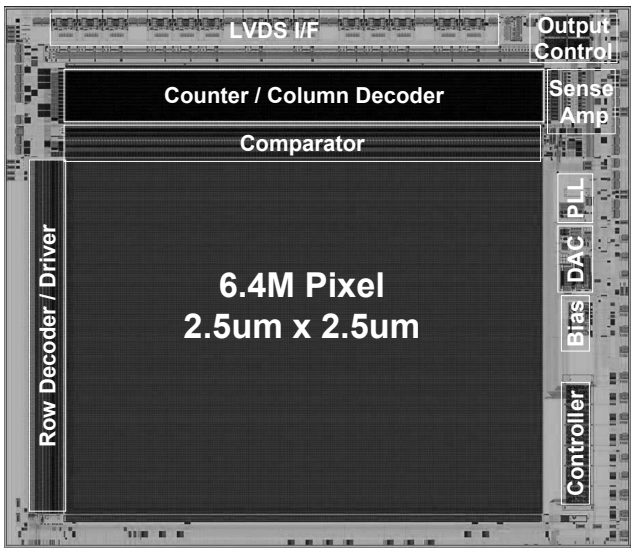

Figure 27.1.7: Chip micrograph.

